3. Binary readout IC for X-ray imaging using silicon strip detector

In this chapter we present multichannel ASIC dedicated for digital imaging using low energy X-rays. The problems discussed previously, like low noise performance, immunity to the switching noise and uniformity of analogue parameters for all channels are essential for the quality of this design and possible future application of such IC. To better understand all requirements and constrains important for this design, we briefly review some aspects connected with silicon strip detectors and possible detector readout architectures.

In various areas of physics, biology and medicine imaging methods using position sensitive detection of X-ray have been developed [66].

There are basically two types of position sensitive detectors:

- detectors based on charge integration, as photographic emulsions,
- detectors which work in the single photon counting mode.

The imaging techniques using the detectors of the second type are sometimes called as digital imaging. An advantage of single photon counting detectors is essentially an infinite dynamic range contradictory to the integration-type detectors, which usually have problems with a limited dynamic range and so a low contrast of the image.

Among various types of position sensitive detectors the most commonly used are silicon detectors built as matrices of reverse biased diodes processed on common high-resistivity substrate. The sensitive area can be divided into individual diodes of the shapes as required by the experiment. In order to make an effective use of such detectors, each sensitive element (diode) should be connected to an individual electronic readout channel. Given relatively low level of the signals generated in silicon by X-rays, a sophisticated analogue processing of the signal is required in order to achieve a reasonable signal-to-noise ratio. At this point one should note that imaging techniques based on the CCD pixel devices are advanced and widely used. However, the applications of standard CCD to the X-ray detection require the use of converters of X-rays to visual photons. The incident X-rays and the generated visual light photons are scattered in the converter material and these scattering effects limit the spatial resolution of such devices. Therefore, direct detection of X-rays by fully depleted thick silicon diodes built on high-resistivity substrate is very attractive for imaging applications.

3.1. Silicon strip detector

A typical silicon strip detector is an array of reverse biased junction diodes made on high resistivity (1–10 kΩ·cm) silicon substrate 250–500 μm thick. The diodes are shaped

according to the geometrical requirements of the experiment concerning the area to be imaged and the spatial resolution (Fig. 3.1). A charged particle or photon passing through the detector loses its energy. The generated charge moved by the electric field inside the detector induces currents in the strips. Reading these current pulses one can reconstruct the position of incident particle and obtain one dimensional image.

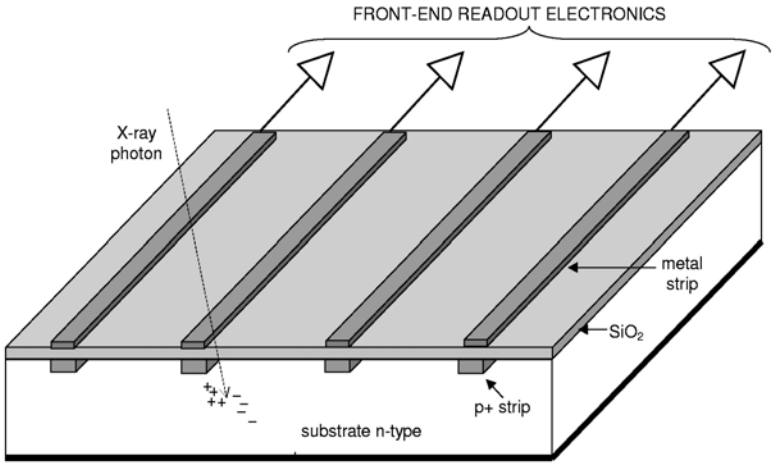


Fig. 3.1. Simplified view of silicon strip detector (AC coupled)

An effective use of standard silicon strip detectors for X-ray measurements is limited to the energy range from about 5 keV to about 20 keV. These limits are not distinct and in some applications silicon detectors can be used also for X-ray of energies outside this range. In the energy range under consideration the photoelectric effect is the dominant mechanism responsible for the photon absorption. The generated photoelectron deposits its energy in a very small volume (practically in a single point), generating hole-electron pairs. Keeping in mind that the conversion factor for silicon for generating electron-hole pairs is 3.6 eV/e-h, a single 5 keV photon produces about 1400 electron-hole pairs which are then collected by the readout electrodes in about 20 ns. To obtain a reasonable signal-to-noise ratio, above 10, the readout electronics should have the equivalent noise charge below 140 el. rms. This is about the practical limit one can achieve in a complex multichannel system working at room temperature.

Concerning the upper energy limit there are two effects which should be taken into account:

- reduction of the detection efficiency due to a finite thickness of the detector,
- degradation of the intrinsic spatial resolution due to Compton scattering and the effect of parallax for incident angles different from the 0 degree.

The main parameter of the position sensitive system is its spatial resolution determined by:

- intrinsic spatial resolution of silicon resulting from the interaction of photons with the detector material,

– strip pitch of the detector,
– signal to noise ratio of the readout system.

One can find the details on intrinsic spatial resolution of silicon strip detectors for X-rays of low energy range in [2]. The strip pitch of the detector used for such application is usually in the range of 50 μm to 200 μm.

Concerning the signal-to-noise ratio of the readout system three parameters of silicon strip detectors are important:

– shot noise of the detector leakage current (per one strip),
– thermal noise of the bias resistor (AC coupled detectors only),
– total capacitance per one strip (bulk capacitance and interstrip capacitance).

3.2. Detector readout architecture

A typical signal processing channel is shown in Figure 3.2. A current signal generated in the silicon strip detector is integrated in a charge sensitive preamplifier. At the output of the preamplifier one obtains a voltage step with an amplitude proportional to the total charge generated in the detector. The voltage step is fed to the main amplifier, called a shaper, which provides the pulse shaping according to the timing requirements and the filtration of noise to maximise the signal to noise ratio.

Further processing of the shaped signal can be done in two possible ways. The first one is based on what is called a binary readout architecture. In that case the comparator detects the presence of the signal of amplitude above the preset threshold and in the response provides 1-bit yes/no information. The second way of processing the shaped signal employs what is called an analogue readout architecture, where the amplitude of the signal corresponding to each individual photon is measured and this information is stored and used for off-line processing.

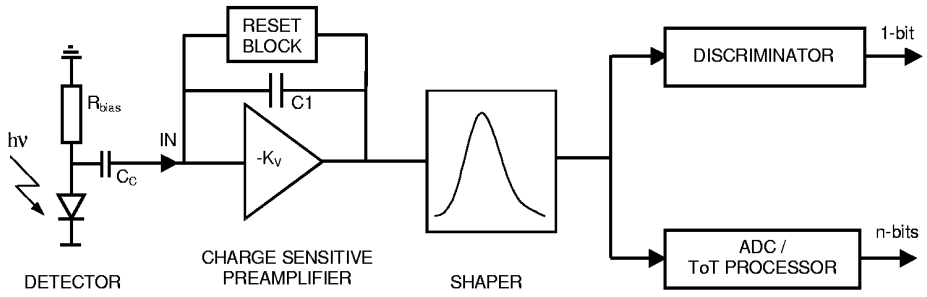


Fig. 3.2. Principal block of a detector readout system

Regardless of the overall complexity of the IC, the basic problems associated with the noise optimisation of the signal processing channel are similar as in conventional circuits and are discussed in details in section 3.4. Here we concentrate on more general aspects of readout architecture as possible solutions for the reset block in the preamplifier and on further signal processing at the shaper output.

After integration of the current pulse in the preamplifier, the feedback capacitor C1 should be discharged by the reset block (Fig. 3.2) during a short period of time to prevent the piling up of pulses in the preamplifier. There are two basic techniques used for discharging the feedback capacitance, continuous discharge and switch reset. Continuous discharging can be completed either by a resistor in parallel to the capacitor or by a controlled current source. In either case the discharging component contributes to the parallel noise at the preamplifier input. In order to limit this noise source, one should use a large value resistor or a low discharging current but then the decay time constant of the preamplifier output signal is long and one still faces limitations of the pulse rate due to the piling up.

Another way of discharging the feedback capacitor is to employ a switching circuit which periodically resets the capacitor. Such a solution is commonly used in ASICs for the readout of silicon strip detectors in the particle physics experiments on the collider, in which, if the signals appear, they appear synchronously in all the channels. The trigger signal for discharging the capacitors is provided by the central clock of the experiment. In X-ray measurements the signals appear randomly in time and independently in each channel. After receiving a signal from the strip, the circuit has to generate the trigger signal for discharging the capacitor. In order to generate such a trigger signal one needs to implement a threshold discriminator in every channel. Various schemes used for discharging the feedback capacitor are discussed in detail in [67].

Further signal processing at the shaper outputs in the multichannel chip depends strongly on the specific requirements of the foreseen applications. Some possible diagrams of further signal processing are shown schematically in Figure 3.3. In various imaging techniques employing monoenergetic X-rays it is sufficient to measure spatial distributions of the X-rays of energies above a given threshold or within a given energy window. For such applications one can use the binary readout architecture (see Fig. 3.3a). In this architecture each channel of the front-end electronics is equipped with an amplitude discriminator which generates 1-bit information in response to each signal above a given threshold. The information delivered by a strip detector is suppressed to the minimum already in the front-end circuit. Binary information can be easily stored in the integrated circuit separately for each channel, which allows one to cope with high rates of the X-rays as each channel works independently. This is a significant advantage in systems comprising hundreds or thousands of channels. ASICs with the binary readout architecture have been developed and used successfully to read out silicon strip detectors in diffractometry measurements [41,68].

The signal amplitude at the shaper output contains information about the charge generated in the detector, which can be useful for spectrometric experiments or to improve the spatial resolution in position measurements. Although measuring the amplitudes of the signals in the analogue architecture has some advantages, it is very difficult to implement this scheme in systems comprising hundreds or thousands of detection elements. As today, it is not feasible to integrate an individual high resolution analogue-to-digital converter (ADC) in each channel of the front-end ASIC.

The constraints are associated with the total area of an IC and with the power consumption. However, if the requirements concerning the resolution of the ADC are not very demanding (6 to 8 bits), one can implement a simple low resolution ADC in each channel. One of the proposed solutions is based on what is called time-over-threshold (ToT) method. Otherwise one has to multiplex some numbers of channels into a single ADC, which can be either integrated in the front-end ASIC or can be an external device.

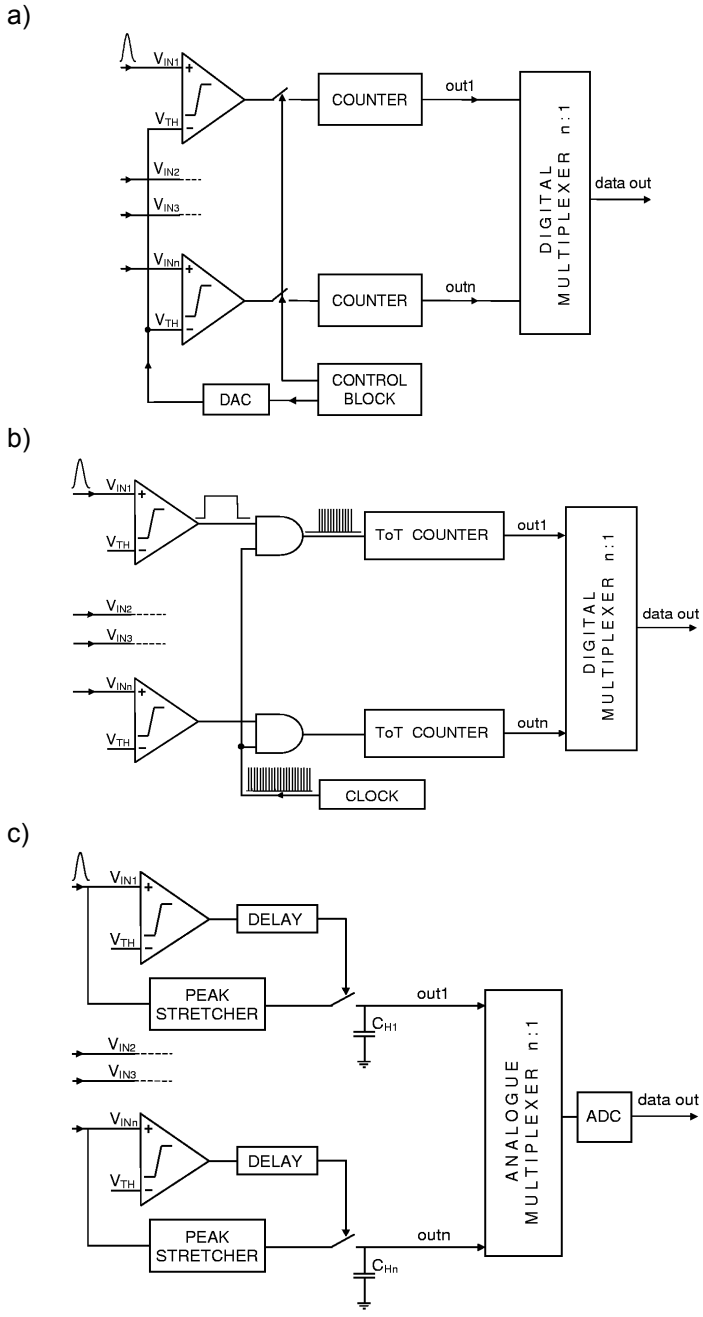


Fig. 3.3. Three possible schemes of readout at the shaper output: a) binary architecture; b) analogue architecture employing time-over-threshold method; c) analogue architecture employing multiplexing of analogue signals

In the time-over-threshold method [69, 70] the analogue signal from the front-end circuit is applied to a simple threshold discriminator as in the binary scheme. The idea is shown schematically in Figure 3.3b. The duration time of the discriminator response is measured in a simple way by counting pulses from a clock generator over the period equal to the duration of the discriminator response. The width of the discriminator pulse depends on the relative amplitude with respect to the threshold and so contains some information about the signal amplitude. A response function of such a system is non-linear; however, it is well defined for a given pulse shape from the shaper circuit. The main advantage of such a scheme is its simplicity and low power consumption that allows one to implement it in every channel. However, one can easily notice basic limitations of this scheme, e.g. the measurement range limited by the discrimination level, low accuracy for small signals just above the threshold, sensitivity to the time jitter of the discriminator, especially for low amplitudes. The scheme has been implemented in an ASIC used for the readout of silicon strip detectors in the particle physics experiments. Let us note, that in the scheme shown in Figure 3.3b, it is not possible to store data for more than one event in the front-end ASIC. Thus, one needs either to multiplex all the channels into one serial output, or elaborate a scheme of sparse readout [71].

A fully analogue readout scheme, employing a true ADC, is shown schematically in Figure 3.3c. In this scheme each channel is equipped with a peak detector and a sample and hold (S&H) circuit. Such schemes are commonly used in synchronous experiments where an external trigger signal, common for all the channels, is available. In applications to X-ray measurements one needs to implement a threshold discriminator in each channel to generate a trigger signal for the S&H circuit in each channel independently. The analogue signals from a certain number of channels are then multiplexed into one ADC which, in most cases, is an external device, although one can consider integrating it in the front-end ASIC. In such a scheme the intensity of X-rays is limited by the multiplexing rate and the speed of the ADC and not so much by the pulse shaping in the front-end circuit. There is an obvious trade-off between the intensity of X-rays and the number of channels multiplexed into one ADC. In experiments with high X-ray intensity one can reduce the number of channels per ADC and increase the number of ADCs in the system.

Another aspect specific for such an architecture concerns the control of the multiplexer and the ADC operation. One can either run the multiplexer and the ADC continuously [72], allowing for some probability of the pile-ups in the S&H circuits, or trigger the multiplexer and the ADC upon a signal occurring in the detector [73]. The most commonly used scheme is based on OR gate taking inputs from all the channels. Then each signal occurring in any of the channels triggers the readout sequence.

One should keep in mind the fact that the readout ASICs with architectures, as shown in Figure 3.3, are custom designed and for a given number of channels in one IC, and for a given readout scheme there is no possibility to reconfigure the IC topology. The progress in the VLSI technology opens new possibilities for integrating more functions in single ASICs, however, they become even more specific for given applications. Using submicron CMOS processes one can easily imagine the integration of an ADC in the front-end ASIC or even several ADCs in one ASIC to increase the throughput of data. Another trend of the development, particularly important for analogue readout architectures, is to integrate in the front-end ASICs analogue memory buffers that can serve as derandomizers. Amplitudes of signals occurring randomly in time are stored in such a buffer and read out with a constant

rate adjusted to speed of the multiplexer and the ADC. Providing that the derandomizing buffer is sufficiently deep for complete removal of statistical fluctuations from trains of incoming pulses, one can increase the intensity of X-rays by an order of magnitude for the same multiplexing and data conversion rate. Several derandomizing schemes for analogue memories have been developed for ASICs used in the particle physics experiments [74], and the first implementation to X-ray measurements has been reported [75].

3.3. Binary readout architecture of RX64 IC

In the position sensitive detection of X-rays, the spatial resolution is significantly limited by Compton scattering of photons in the semiconductor material and by the diffusion of generated charge carriers during their transport in the sensitive volume of the detector [2,76]. There is essentially no profit from using the pulse height information for the evaluation of the centre of gravity of a charge collected on several strips. Therefore the presented here RX64 IC for the readout of the silicon strip detector for the X-ray imaging has been based on the binary architecture. The IC is dedicated to the Roentgen diffractometry which needs a fast and cheap one-dimensional position sensitive imaging system working at room temperature and providing spatial resolution of about 100 μm. Projects with similar objectives have been undertaken recently by other groups [77, 78, 79].

The block diagram of the complete RX64 IC is shown in Figure 3.4. The chip comprises five basic blocks: analogue front-end channels, counters, an input-output block, a control block and a calibration circuit with digital to analogue converters (DACs).

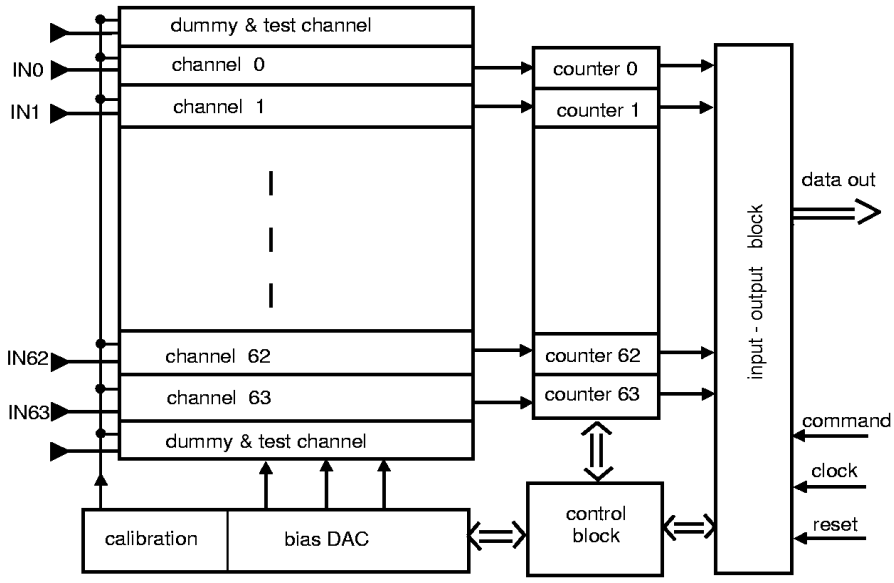


Fig. 3.4. Block diagram of RX64 chip

The front-end channel is responsible for the extraction of signal from the silicon strip detectors, filtering of noise and shaping of the analogue voltage signal. In this case each front-end channel is equipped with a comparator providing discrimination of the analogue signal at a given level. Due to statistical nature of X-ray sources the signals at the output of the discriminator appear completely randomly in time and are stored in 20-bit asynchronous counters. The counters are grouped in blocks of 8 channels each and the data from each block can be read out through tristate outputs.

In a single chip 64 channels have been integrated. They can simultaneously process signals and store data from 64 elements of a silicon strip detector. Such architecture provides fully parallel signal processing, including data storage, from all strips. It is suitable for high counting rate applications, since the amount of data to be handled is already minimised in the front-end part. In addition to the basic functions which control the data storage and the readout, the control block provides the settings of the DACs which are used in the front-end block for biasing the analogue circuits and for the control of the internal calibration circuit. The chip is controlled by commands delivered from an external controller through a serial link. The control block receives the commands, decodes and executes them by sending the control signals and data to other blocks.

3.4. Front-end circuit

Although in the binary readout architecture the front-end channel is ended up with a discriminator the signal-to-noise ratio remains one of the most critical problems to be solved. A typical plot of number of counts at the discriminator output as a function of threshold voltage level is shown in Figure 3.5a. For the low threshold values (in Fig. 3.5a below 50 mV) a rapid increase of counts is observed. This is due to the noise at the discriminator input which for the low threshold level switches on the comparator and contributes to the total number of counts. By differentiating the total number of counts vs the threshold level, one obtains what is called pulse height spectrum shown in Figure 3.5b. The noise and the signal smeared by the noise are clearly visible. Sufficient separation between the noise level and the signal level is required in order to provide high detection efficiency and limited noise count rate. For a system with white input noise and a first order band-pass filter the noise count rate at the comparator output is given by the formula [80]

$$f_n = f_0 \exp\left(-\frac{V_{TH}^{\ 2}}{2\sigma_n^{\ 2}} \right) \tag{3.1}$$

where:

- f_0 – noise count rate at zero threshold level,
- V_{TH} – comparator threshold,
- σ_n – voltage noise rms at the comparator input,
- τ – time constant of the filter.

In order to keep the noise count rate at a negligible level, it is required for a typical detection system that the comparator threshold is set at least at a level of $3\sigma_n$.

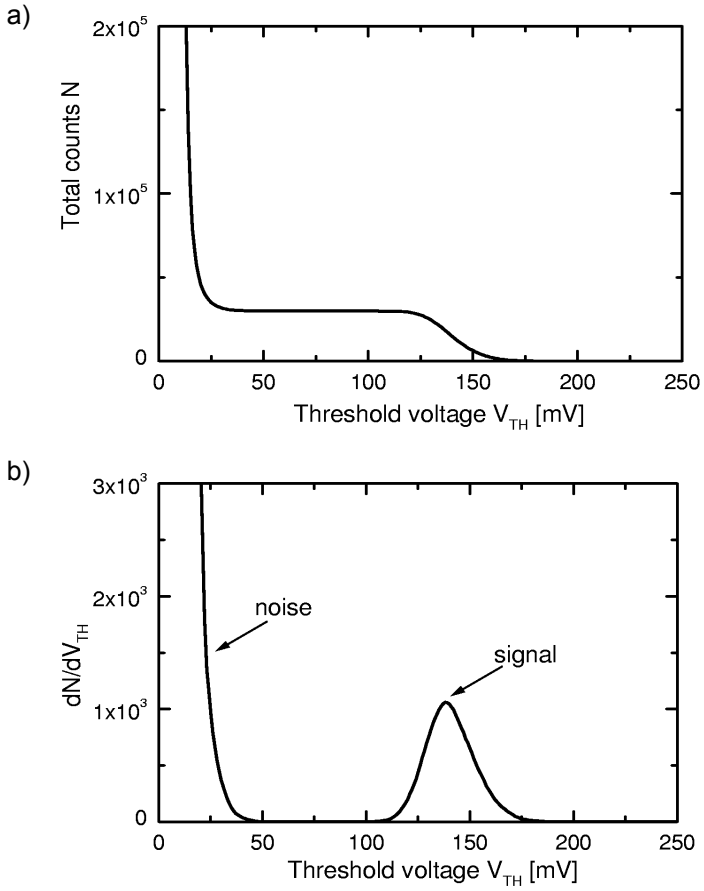


Fig. 3.5. Counts at the discriminator input vs threshold level for a given acquisition time: a) total number of counts; b) differential pulse height spectrum

On the other hand, the comparator threshold should be low enough to provide full efficiency for the signals. Since the signals are smeared by noise around the mean value another margin of $3\sigma_n$ for the threshold setting is needed. Then, taking into account some additional effects such as fluctuation of charge generated in silicon detectors, charge division between neighbouring strips and channel-to-channel variations of amplifier gain and comparator offset for a multichannel system, one arrives at a conclusion that a signal-to-noise ratio about 10 is required. In addition the immunity to switching noise is critical problems for such systems.

The block diagram of the single front-end channel of RX64 chip is shown in Figure 3.6. The channel is built of three basic blocks: a charge sensitive preamplifier, a shaper and a discriminator. The input signal is considered as a charge signal which is a proper approach since the primary task of the front-end system is to convert the total charge generated in the detector by radiation into the voltage signal proportional to the

particle or photon energy deposited in the detector. For the silicon strip detectors the typical charge collection time is of the order of 20 ns and the details of the actual current pulse shape can be ignored.

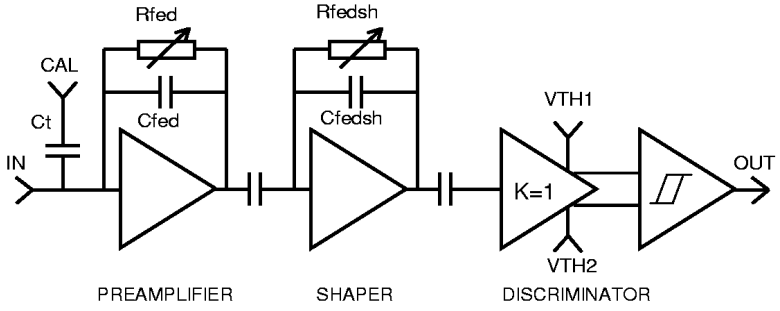


Fig. 3.6. Block diagram of the single front-end channel

The performance of the front-end system is described by three basic parameters:

- the charge gain defined as the ratio of the voltage signal at shaper output to the input charge,
- the ENC (Equivalent Noise Charge) as the charge applied to the input in a form of a short δ-like current pulse which gives at the output a signal amplitude equal to the rms value of noise σ_n,
- the maximum count rate.

Let us analyse noise performance of the front-end system comprising a charge sensitive preamplifier (integrator) followed by a band-pass filter (shaper). The noise performance of such a system can be analysed using an equivalent input voltage noise generator and an equivalent input current noise generator. The voltage noise is dominated by the thermal and flicker noise of the input transistor of the charge sensitive preamplifier and according to formulae (2.3), (2.11) and (2.14) can be expressed as

$$\frac{\overline{dv_n^2}}{df} = \frac{8}{3}kT\frac{1}{g_{m1}} + \frac{K_f}{C_{ox}^2}\frac{1}{W_1 L_1}\frac{1}{f} \tag{3.2}$$

where:

g_{m1} – gate transconductance of the input transistor ,
W_1, L_1 – width and length of the input transistor.

The current noise is associated with the detector leakage current I_{DET} (shot noise) and the thermal noise of the detector bias resistor R_{bias} and feedback resistor R_{fed} in the preamplifier, so the power spectral density is given by

$$\frac{\overline{di_n^2}}{df} = 2qI_{DET} + \frac{4kT}{R_{bias}} + \frac{4kT}{R_{fed}} \tag{3.3}$$

The equations (3.2) and (3.3) can be rewritten in the shorter forms as

$$\frac{\overline{dv_n^2}}{df} = a + \frac{b}{f}$$
$$\frac{\overline{di_n^2}}{df} = c \tag{3.4}$$

where:
a – white component of the voltage noise,
b – flicker component of the voltage noise,
c – white component of the current noise.

In order to find the ENC of the detector system one needs to calculate the rms value of noise at the shaper output. Knowing the charge gain of the system the equivalent noise charge can be expressed as [81, 82]

$$\mathrm{ENC} = \sqrt{a\frac{F_v C_{in}^2}{T_p} + bF_{vf}C_{in}^2 + cF_i T_p} \tag{3.5}$$

where:
C_{in} – total input capacitance including the gate capacitance of the input transistor, silicon detector capacitance and any stray capacitance of the connection between the silicon strip detector and the readout chip;
T_p – peaking time, i.e. the time at which the signal at the filter output reaches the maximum; for a simple CR-RC band-pass filter the peaking time T_p is equal to the time constant of the filter $\tau = RC$;
F_v, F_{vf}, F_i – constants dependent on the filter type.

Three immediate observations based on formula (3.5) are important for the optimisation of the front-end circuit, viz.:
- contribution of the input voltage white noise to the ENC is proportional to the total input capacitance and inversely proportional to the square root of the peaking time,
- contribution of the input current noise is independent of the input capacitance and proportional to the square root of the peaking time,
- contribution of the input voltage flicker noise to the ENC is proportional to the total input capacitance and independent of the peaking time.

One can now optimise the front-end system taking into account various requirements and constraints implied by a particular application. There are two parameters, which are determined by the detector geometry and vary over wide ranges. They are detector capacitance and detector leakage current. Both parameters are proportional to the strip length and the interstrip capacitance dominates for small strip pitch. Another detector parameter, which varies over wide range, is the leakage current. In the first approximation the leakage

current per strip is proportional to the space charge volume corresponding to a given strip and so it is proportional to the strip area. The leakage current is, in addition, a strong function of temperature and lowering the temperature is a way to reduce the leakage current and the shot noise associated with it. From formulae (3.3) and (3.5) it is obvious that the detector bias resistor R_{bias} and feedback resistor R_{fed} should be relatively high not to contribute to the noise. The high value of R_{bias}, in the range of tens of MΩ, can be obtained by using for example FOXFET structure to bias the detector [83]. In the case of R_{fed}, the situation is more complicated, because the high value of this resistor limits the count rate performance of the system.

The next parameter, which can be considered as an input to formula (3.5), is the peaking time T_p. If, for example, there is no constraint on the peaking time, as for any low rate experiment, one can find an optimum peaking time for other given parameters, voltage and current noise spectral densities and detector capacitance [82]. However, in many applications high counting rate capability is a serious requirement which has to be taken into account as a limitation for the maximum allowable peaking time.

3.4.1. Preamplifier

In the case of RX64 chip the preamplifier is designed to work with DC coupled detectors and it should be able to sink a detector leakage current in the range from a few pA up to a few nA through the feedback loop. The preamplifier is based on a folded cascode configuration built of transistors M1, M2 and M3 (Fig. 3.7).

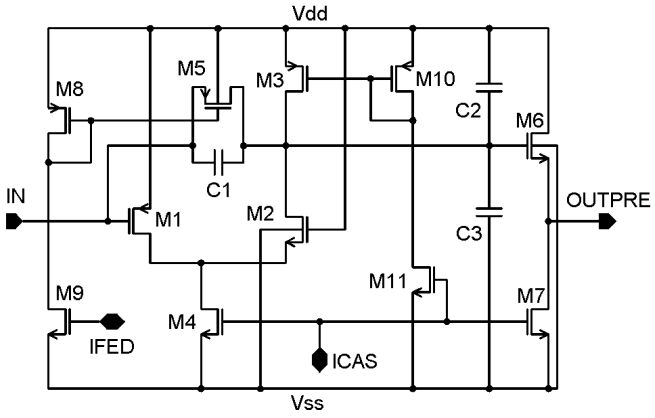


Fig. 3.7. Schematic diagram of the preamplifier

The open loop gain of such configuration is determined by the ratio of currents in the left and the right branch of the folded cascode, by the sizes of the input transistor M1, the load transistor M3 and by the total current I_{DS1} in the input transistor according to the formula (see Appendix I)

$$K_v = -\frac{\sqrt{2\mu_p C_{ox} W_1/L_1}}{\lambda_3} \frac{A_I}{\sqrt{I_{DS1}}} \tag{3.6}$$

where:

$\mu_p C_{ox}$ – transconductance parameter of the input transistor M1,
W_1 , L_1 – width and length of the input transistor M1,
λ_3 – channel length modulation parameter of the load transistor M3,
I_{DS1} – drain-source current of transistor M1,
A_I – ratio I_{DS1}/I_{DS3} of the currents in transistors M1 and M3.

The ratio A_I of the currents in the two branches is about 30. The other parameters, which define the open loop gain, are driven mainly by noise optimisation. The input transistor has to be optimised according to the actual detector capacitance taking into account the fact that transistors with the minimum gate length show an excess noise due to short channel effects. For the foreseen strip capacitance in the range from 2 to 5 pF a PMOS transistor of W_1/L_1 = 400μm/1.5μm has been chosen as an input device. A PMOS device has an advantage over an NMOS one due to lower 1/f noise, although it has also a drawback due to a higher current needed to obtain the required transconductance. In this solution the transconductance of M1 is about g_{m1} = 3.4 mA/V for the current I_{DS1} = 500 μA. The open loop gain of the input stage is about 5000 V/V.

The feedback loop in the preamplifier is formed by the capacitor C1 of 200 fF and the channel conductance of transistor M5 working in the linear region. The preamplifier response to a δ-like current pulse carrying charge Q is given as (see Appendix II)

$$v_{outpre}(t) = -\frac{Q}{C_1}\left[\exp(-t/\tau_1) - \exp(-t/\tau_2)\right] \tag{3.7}$$

where the time constants τ_1 and τ_2 are given by

$$\begin{aligned} \tau_1 &= \frac{C_1}{g_{ds5}} \\ \tau_2 &= \frac{(C_2 + C_3)(C_{det} + C_{gs1})}{g_{m1} C_1} \end{aligned} \tag{3.8}$$

where:

g_{m1} – gate transconductance of transistor M1,
g_{ds5} – source-drain conductance of transistor M5,
C_1, C_2, C_3 – values of the corresponding capacitors shown in Figure 3.7,
C_{gs1} – gate-source capacitance of transistor M1,
C_{det} – detector capacitance.

The time constant τ_1 is responsible for the signal decay and is rather long, of the order of a few tens of μs. The time constant τ_2 is responsible for the rise time at the preamplifier output. It is in the range from a few tens of ns up to hundreds of ns depending on the detector capacitance C_{det}. The time constant τ_2 has been made intentionally longer by adding the capacitors C2 and C3 of 5 pF each. This time constant introduces a significant pole to the overall shaping function of the circuit. The source follower M6–M7 forms the preamplifier output stage.

Transistor M5 has W_5/L_5 = 2μm/384μm and works as a high value feedback resistor. It provides the bias voltage to the gate of transistor M1, the current to the detector strip and a discharge path for the feedback capacitor C1. The transistor operates in the linear region, and high output resistance, of the order of tens of MΩ, has been achieved by the proper transistor geometry with a very long channel. This resistance is large enough so that it does not represent any significant load for the output of the folded cascode. The operating point of this transistor is set by V_{GS} of transistor M8, which is controlled by the reference current IFED. The channel resistance of transistor M5 contributes to the parallel noise at the preamplifier input and from that point of view it should be high. This resistance also determines the time constant τ_1 of the pulse tail at the preamplifier output. Thus, one has to make a compromise between the noise performance and the dead time of the circuit. The detector leakage current, if relatively large, puts another limitation on the value of the feedback resistance.

The biasing scheme of transistor M5, which is responsible for the time constant of the feedback network, is essential for the operation of the circuit with a high rate of input signals. Due to piling up of pulses at the preamplifier output the DC level moves and changes the drain-source voltage of transistor M5 by ΔV_{DS}, while the gate-source voltage V_{GS} and the small signal output resistance of this transistor remains practically unchanged. The actual value of the current discharging the feedback capacitor depends on the ΔV_{DS} voltage. This mechanism provides a dynamic control of the voltage across the feedback capacitance, depending on the rate of input signals, and prevents the saturation of the preamplifier. At the expense of some additional fluctuation of gain, which at the end contributes to the energy resolution, the circuit can work with much higher rates of signals, compared with the one, that could be expected from the small signal analysis.

3.4.2. Shaper

The shaper is built of the coupling capacitor C4 of 15 pF and the integrator employing the folded cascode configuration M14–M16 with the feedback network M18 and C5 of 100 fF (Fig. 3.8).

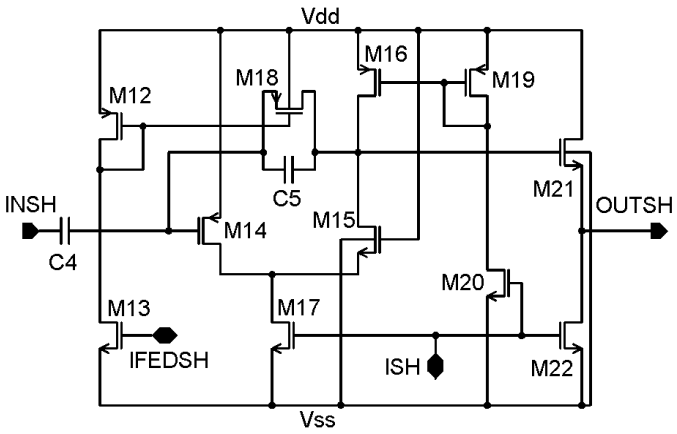


Fig. 3.8. Schematic diagram of the shaper

The frequency response of the shaper is given by (see Appendix III)

$$K_v(s) \approx \frac{sC_4\left(sC_5 - g_{m14}\right)}{s^2C_4\left(C_{os} + C_5\right) + sg_{m14}C_5 + g_{m14}g_{ds18}} \tag{3.9}$$

where:

g_{m14} – gate transconductance of transistor M14,
g_{ds18} – source-drain conductance of transistor M18,
C_{os} – total capacitance to the ground seen from the drain of transistor M16,
C_4, C_5 – values of the corresponding capacitors shown in Figure 3.8.

This response has two zeros z_1 and z_2

$$\begin{aligned} z_1 &= 0 \\ z_2 &= \frac{g_{m14}}{C_5} \end{aligned} \tag{3.10}$$

with z_2 being negligible as located in the very high frequency region. The two poles p_1 and p_2 are real and negative value. Since $|p_1| << |p_2|$, the poles can be written as

$$\begin{aligned} p_1 &\approx -\frac{g_{ds18}}{C_5} \\ p_2 &\approx -\frac{g_{m14}C_5}{C_4\left(C_{os} + C_5\right)} \end{aligned} \tag{3.11}$$

The poles, being real, guarantee that the pulse response of the shaper decays asymptotically without undershoots. Separation of the preamplifier from the shaper by the source follower M6–M7 makes the values of the shaper poles independent of the detector capacitance.

The shaper response to a unity voltage step is given as

$$v_{outsh}(t) = -\frac{C_4}{C_5}\left[\exp\left(-|p_1|t\right) - \exp\left(-|p_2|t\right)\right] \tag{3.12}$$

The bias currents in the shaper are controlled via the current mirrors by the reference currents ISH and IFEDSH. This solution offers a possibility to control the g_{m14} and g_{ds18} and also in this way the rise and the fall time of pulse at the shaper output.

3.4.3. Discriminator

A single-ended configuration of the preamplifier and the shaper results in a significant channel-to-channel offset variation. On the other hand, a practical solution for the front-end

chip is to use a common threshold for all 64 discriminators in one chip. In order to eliminate the offset and the base line shift at the shaper output, the discriminator is AC coupled to the shaper (Fig. 3.9). A drawback of this solution is a baseline shift for high count rates, about 6 mV for 100 kHz rate of signals corresponding to the X-ray energy of 8 keV. This value, if compared with the signal amplitude about 160 mV, is fully acceptable for this particular counting applications.

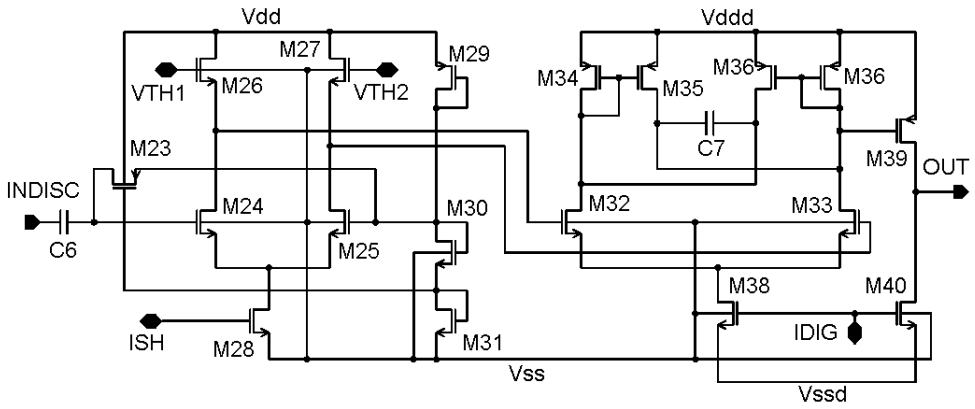


Fig. 3.9. Schematic diagram of the comparator

In addition, a fully differential scheme is employed in the comparator design. The differential stage M24–M27 of approximate unity gain is used to apply a differential threshold voltage to the comparator built of transistors M32–M38. The differential scheme for setting the comparator threshold (VTH1–VTH2) allows one to use the circuit either for positive or for negative input signals. The hysteresis of the comparator is controlled by an external current IDIG. In order to reduce the effect of the comparator switching on the front-end, the comparator response is purposely slowed down by a capacitor C7 of 200 fF. In addition, the power supply rails are cut after the differential pair so that the comparator has a separate Vddd and Vssd power rails.

3.4.4. Matching and immunity to the switching noise

The main challenge from the point of view of the front-end design is to integrate the counters and all digital control logic on the same die without compromising analogue performance. In the present design there are 64 front-end channels, so in this section, we focus our attention on two problems which are absolutely critical in such a multichannel mixed-mode chip, namely:

- gain and offset matching for all channels,
- immunity to digital noise.

Due to statistical nature of X-rays the signals appear in the strips of the detector, and so in the electronic channels, completely randomly in time. This feature requires using a continuous time comparator for the discrimination on the signal amplitude and excludes

the possibility of applying an auto-zero-technique. Since we have decided to use a common threshold applied to all 64 channels in the chip, special attention has been paid to minimise the channel-to-channel variation of gain and offset. At this point one should note that another possible solution of the problem by implementing individual offset correction in every channel has been successfully tried in another design [54].

In order to reduce the channel-to-channel offset spread, AC coupling has been implemented between the preamplifier and the shaping amplifier, as well as in front of the discriminator. Furthermore, the circuit following the shaping amplifier is designed in fully differential mode. The differential pair in front of the discriminator has a gain close to 1 and its main function is to generate a differential threshold for the comparator. In this design the requirement concerning the speed of the comparator is rather relaxed because the counting rate of the overall channel is limited by the pulse duration time in the shaping amplifier, which is in the range of microseconds. Therefore one can use fairly large devices in the matching sensitive circuits. The differential sections in the discriminator have been laid out in the common centroid geometry, with symmetrical surrounding and no metal layer overlaps. Provided that the gain in the preamplifier and the shaper stage is high enough the chosen solution allows one to keep the rms value of the channel-to-channel offset spread much lower than the rms value of noise at the input of the comparator.

The gain of the preamplifier (Fig. 3.7) and the shaper (Fig. 3.8) is determined by the components of the feedback loop circuits and coupling capacitor C4 of 15 pF. The capacitors C1 and C5 of the value 200 fF and 100 fF respectively are designed as poly-poly capacitors following the layout rules recommended for precision capacitors [84]. The tuneable feedback resistors R_{fed} and R_{fedsh} (Fig. 3.6) of the order of tens of MΩ are realised as long PMOS transistors working in the linear region. The dimensions of these feedback transistors are W_5/L_5 = 2μm/384μm for the preamplifier and W_{18}/L_{18} = 2μm/84μm for the shaper and their gate-source bias voltages are controlled by the internal DACs implemented in the chip. Using such large transistors in parallel with small capacitors in the feedback circuits requires proper simulation of the circuit. In order to evaluate correctly the effect of the distributed channel-to-well capacitance of such long PMOS transistors, during simulation the long transistors have been split for a series of N, up to 6, shorter transistors. Although in an n-well process the matching performance of PMOS transistors is usually worse than those of NMOS ones [42], PMOS devices as the feedback resistors have been used for their lower 1/f noise [85], larger small signal drain-source resistance and higher immunity to the switching noise [31, 56].

In addition to the core part of the front-end block comprising 64 channels (Fig. 3.4), two additional dummy channels have been added on each side of the chip in order to guarantee good matching of the active channel 0 and 63 at each edge of the chip. Distribution of the power supplies and reference signals is another important problem for the matching in multichannel systems and it is discussed in detail in chapter 3.8.

The analogue part of the chip may work satisfactorily when fabricated as a separate die, however, some deterioration of the analogue performance is usually observed when digital blocks are added [22]. The substrate of the technology used is composed of an epitaxial layer grown on heavily doped bulk substrate. Low resistivity substrate is a very good conductor for the distribution of substrate noise and isolation techniques by guard rings are not so effective as for a lightly doped substrate [23]. A remedy for this problem could be fully differential front-end circuit with sufficiently high CMRR and good PSRR. However,

in this case the driving requirement of low noise prohibits such a solution in the input stage of the front-end channel. The preamplifier and the shaper have been designed as a single-ended stages using folded cascode configuration. Obviously, the input transistor is the most sensitive component. In order to reduce the possible injection of substrate noise to the input of the preamplifier a PMOS transistor is used as an active device in the input stage. With this configuration the n-well can be used as a shield from substrate. In order to ensure effective functioning of such a shield rings of contacts are placed around the transistors and the contacts are tied to the analogue high power supply voltage Vdd. The load current sources have been made as NMOS transistors referred to the substrate potential Vss. Each group of the NMOS transistors is surrounded by a local guard ring tied to the Vss. Special attention has been paid to contact the substrate in the proper way, especially near the sensitive analogue part, since it is a critical issue for mixed-mode systems on an epitaxial layer.

The immunity of the discriminator to digital noise is increased by implementing a fully differential architecture of the comparator and by careful designing for matching. On the other hand, the comparator itself is a source of switching noise placed in an immediate vicinity of the sensitive single-ended analogue stages. Due to large transistors used, the comparator has relatively slow transient response which limits, to some extent, the generation of the switching noise while the implemented hysteresis prevents multiple response of the comparator to noisy input signals. The first stage of the discriminator, which converts the single-ended signal into a differential one, is powered from the same power supply lines as the preamplifier and the shaper while the comparator with hysteresis has separate power supply lines Vddd and Vssd connected via dedicated bond pads.

3.5. Digital to analogue converters

The RX64 IC is equipped with three 5-bit and one 8-bit digital to analogue converters. Two of the 5-bit current DACs control the values of the feedback resistance in the preamplifier IFED (Fig. 3.7) and the shaper IFEDSH (Fig. 3.8). The third 5-bit DAC is used in the calibration circuit (see chapter 3.6), while the 8-bit DAC sets the threshold voltage VTH1−VTH2 in the comparator (Fig. 3.9).

The DACs are made using binary weighted current sources. The schematic diagram of the 8-bit DAC is shown in Figure 3.10. The precision of that kind of converter is dependent on how well the current sources M50–M57 can be matched or the degree to which they can be made binary weighted [33]. Also the switch-on resistance of transistors M58–M65 should be kept low for the proper operation of the circuit. The layout of DAC is designed with a special care following the rules for good matching described in chapter 2. The unit current source in DAC is made of the PMOS transistor with the dimensions W/L = 10μm/6μm. The least significant bit (LSB) is build of one unit source, the next significant bit of two unit sources connected in parallel and so on. The whole area occupied by the current sources is surrounded by the ring, which consists of dummy unit current sources. The total area of such DAC together with the reference voltage source is 600 μm × 200 μm.

The reference voltage source used in DAC is built of transistors M45–M49 and a resistor R2. It provides reference voltage independent of the supply voltage. Because of two

possible equilibrium DC operating points [48], a start-up circuit (M42–M44) is needed. Since the RX64 IC works at constant temperature in normal operation, the temperature dependence of the reference source is of second importance.

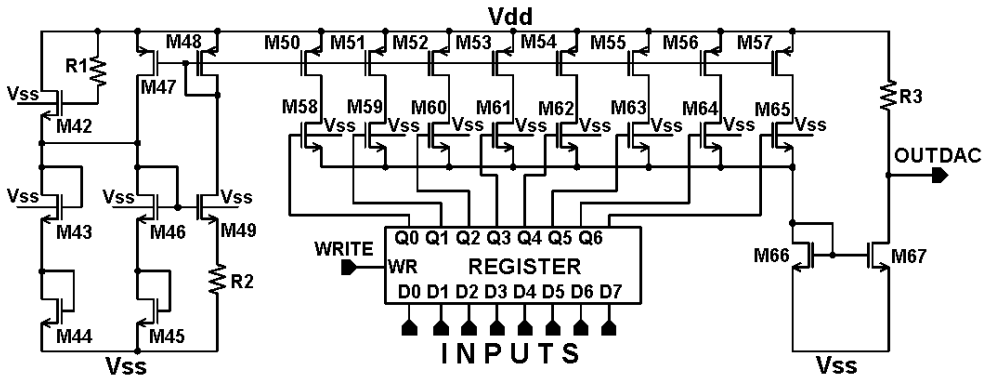


Fig. 3.10. Schematic diagram of 8 bit DAC

3.6. Calibration circuit

As discussed before, the strip detector can be considered as a source of charge signal. Thus, for measuring analogue parameters one has to inject some charge to the preamplifier input. This is typically done by applying a voltage step V_t through a small test capacitor C_t at the input. For $C_t << C_{in}$ the charge injected to the input equals $Q_{inj} = C_t \times V_t$. For this purpose a small capacitor C_t = 70 fF is placed at the input of each preamplifier (Fig. 3.6). A square wave signal of small amplitude applied to the test capacitor generates at the input of the preamplifier short current pulses of well controlled charge.

The main part of the calibration circuit is shown in Figure 3.11.

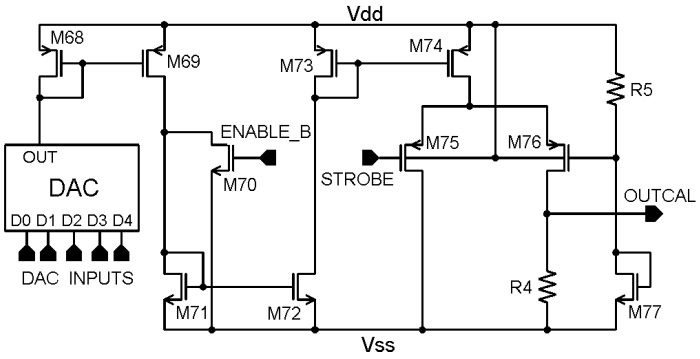


Fig. 3.11. Schematic diagram of calibration circuit

In response to the square wave of 4 V amplitude at the STROBE input that circuit generates a square wave at the output but of small amplitude. The amplitude of the output signal is controlled by 5 bit current DAC in the range from 1 mV to 30 mV. Because of the small amplitude at the output, the problem of the charge injection during switching should be considered carefully. The RX64 has 4 such calibration circuits, each of them delivers test signal to 16 channels simultaneously. The calibration circuit is activated by low signal at ENABLE_B input.

3.7. Digital part

The digital part of the RX64 chip consists of three main blocks: counters, an I/O circuit and a control block. The 64 pseudo-random counters are connected to the outputs of a front-end channel via Schmitt triggers to turn a slowly varying signal from the comparator into a clean digital output signal. The I/O circuit is responsible for the buffering data and for communitation with the external world, while the control block is used not only to control the counters but also the DACs and the calibration circuit in the analogue part of the chip.

3.7.1. Pseudo-random counters

The RX64 chip must discriminate pulses above a given threshold, count them over some period of time and store the data. The counting period depends on the intensity of the measured X-rays and should be programmable. In most imaging applications one has to deal with a large variation of radiation intensity in various detector elements. In order to reduce the effect of statistical fluctuation on the image quality, it is necessary to collect a certain minimum number of counts in the areas of low intensity, while at the same time the number of counts in the areas of high intensities can be higher by several orders of magnitude. In order to be able to measure images with large dynamic range, the capacity of the counters in the RX64 chip has been specified as 20 bits.

The counters in the RX64 chip are based on the concept of a pseudo-random shift register [86]. The 20 bit shift register is configured with a single XOR gate to generate a pseudo-random state sequence. As each state in such scheme corresponds to the number of clock pulses this circuit can be used as a counter. The scheme of the counter structure is shown in Figure 3.12. The 17-th and the 20-th bit of the shift register are XOR-ed and fed back to the register input, so that the period of the pseudo-random sequence is $2^{20}-1$ [87].

Such a concept of the counter circuit has two advantages which are particularly attractive for the multichannel chip. They are simplicity and small size. In the RX64 chip the counting shift register has been designed using semi-dynamic logic which allowed us to achieve a very compact layout. For comparison, in the previous prototype the counter block has been implemented as a separate chip [76] using a very standard counter structure based on T flip-flops resulting in 30 transistors per bit. In the present structure implemented in the RX64 chip one needs only 8 transistors per bit.

The operation of the counters is controlled by four signals: *Gate, ClkEx, A/R* and *Dest/NonDest*. The *Gate* signal is used to open or close the inputs to the counters. When the counter inputs are closed, it is possible to set the counters to the readout mode by setting

"1" on the *A/R* (Accumulation/Read) line. There are two possible modes of the readout procedure, which are controlled by the *Dest/NonDest* (Destructive/Non-Destructive) signal. In the destructive mode, after reading out the content of the counter, all bits in the shift register are set to "1", while in the non-destructive mode the configuration of bits in the shift register remains unchanged. The readout of the counters is performed synchronously with the rate determined by the clock signal *ClkEx* applied externally. The *ClkEx* signal can be used for the test purpose by setting the chip in the accumulation mode. In this mode the external clock signal is directed to the counter inputs. Using this configuration one can perform functionality tests of the counters and the readout controller, as well as evaluate the speed performance of the circuit.

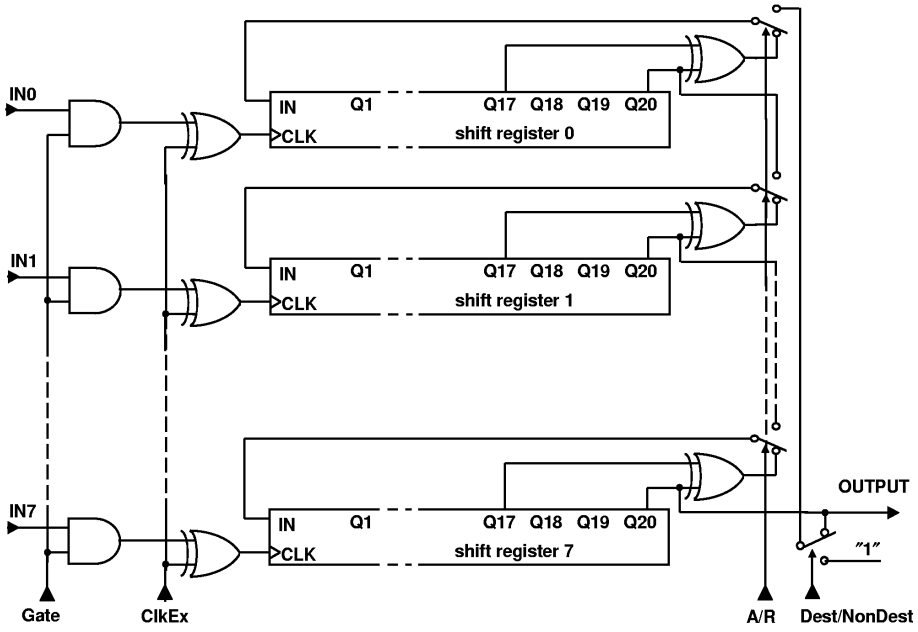


Fig. 3.12. Block of eight counters

A drawback of the scheme based on the pseudo-random shift register is that in order to read out the content of the register one has to stop collecting data. In a continuous experiment this generates what is called dead time, which is a fraction of time over which the data from the detector are lost. In order to minimise the dead time, the counters are grouped in the blocks of 8 counters each, and the data from each block are read out via an 8-bit bus. In order to send the data off the chip, the eight 20-bit shift registers are arranged into a single 160-bit long shift register.

Due to particular requirements for analogue signal processing in the front-end circuit, the maximum rate of data, which can appear at the counter inputs, is about 200 kHz. Thus, from that standpoint of view the speed requirements for the counters are not critical at all, however, due to the dead time issue the minimum clock frequency for the readout logic has been specified as 10 MHz. This number can ensure that for all foreseen measurement configurations the dead time introduced by the counter readout will be negligible.

3.7.2. Control block

In order to minimise the number of external control signals to be delivered to the chip a control block has been implemented. The control block receives commands from an external controller (typically a PC I/O card) via a serial link, decodes them, and generates the signals to the other blocks in the chip. The list of commands is shown in Table 3.1.

Table 3.1
List of commands

Command code	Action
000	OpenGate
001	CloseGate
010	ReadoutDestructive
011	ReadoutNonDestructive
100	CalibrationPulse
101	CounterPulse
110	LoadDac
111	Unused code

In addition to the commands used to control the readout of the counters, there are three other commands implemented: *CounterPulse*, *CalibrationPulse* and *LoadDac.* These commands can be used for test purposes and allow one to test the digital part of the chip, starting from the counter inputs. In response to the *CounterPulse* command, a single pulse is sent simultaneously to all counters through the *ClkEx* line.

Another command which has been implemented for test purposes is the *CalibrationPulse.* In response to this command, a trigger pulse is sent to input STROBE in the internal calibration circuit implemented in the front-end block (Fig. 3.11). Then a current pulse, which simulates the detector signal, is injected into the preamplifier input. This feature allows one to test the overall functionality, including the analogue and the digital parts, as well as to perform detailed measurements of the analogue parameters.

The front-end block contains four different DACs which are used for setting the bias currents, the amplitude of the calibration signal and the threshold in the discriminator. The command *LoadDac* contains, in addition to the command code, 10 bits which define the address of the DAC and the value to be loaded.

3.7.3. I/O circuit

As described before, the RX64 IC comprises analogue front-end circuits which amplify and shape the analogue signals from silicon sensors. Since the signals are very small, a high gain and low noise are critical parameters of the front-end circuit. Both aspects make the circuit potentially very sensitive to the interference from digital signals which can be injected through the silicon substrate. Obviously, the supply voltages for the digital and analogue circuits have to be separated.

In order to minimise the injection of parasitic digital signals to the substrate we have assumed that incoming digital clock and command signals should be differential following the LVDS standard [88]. The input buffers which can receive LVDS signals correctly have been implemented in the chip.

On the other hand, the data outputs are designed in a standard tristate single-ended configuration. The primary reason for this solution is to allow one to connect outputs of up to four chips to a common external bus. This configuration allows one to transmit data to a computer via a single 8-bit bus from up to 4 chips, i.e. up to 256 channels. As the time required for transmitting the data off the chip is usually negligible, compared to the time of data collecting, it is assumed that during reading out the data the input gates will be closed. In this way one avoids a potential problem of analogue signals in the front-end electronics being deteriorated by the injection of parasitic signals from single-ended digital outputs.

3.8. Layout of RX64

The RX64 IC has been designed for the 0.8 μm CMOS technology process by AMS. As the chip contains analogue and digital circuits placed on common epi-type substrate, particular attention has been paid to the layout. A photograph of the chip with the major blocks marked is shown in Figure 3.13. The total area of the die is $2800\times6500\ \mu m^2$ with a major part occupied by the analogue front-end circuits. The counters and the control block occupy an area of about $770\times5400\ \mu m^2$ only.

The floor plan of the chip is determined by the layout of the front-end channels which have to match the strip pitch of the silicon sensor. This particular floor plan imposes some constraints on the layout of the power and ground paths. For all critical paths the extracted resistances of the power supply paths have been taken into account in the simulation. The RX64 chip requires two single-ended supply voltages i.e. 3.0 V for the analogue part and 4.0 V for the digital part. The average current consumption per chip is 45 mA for the analogue and 5 mA for the digital power supply. These numbers result in an average power consumption of 2.5 mW per channel, which is quite low considering the functionality and complexity of the design.

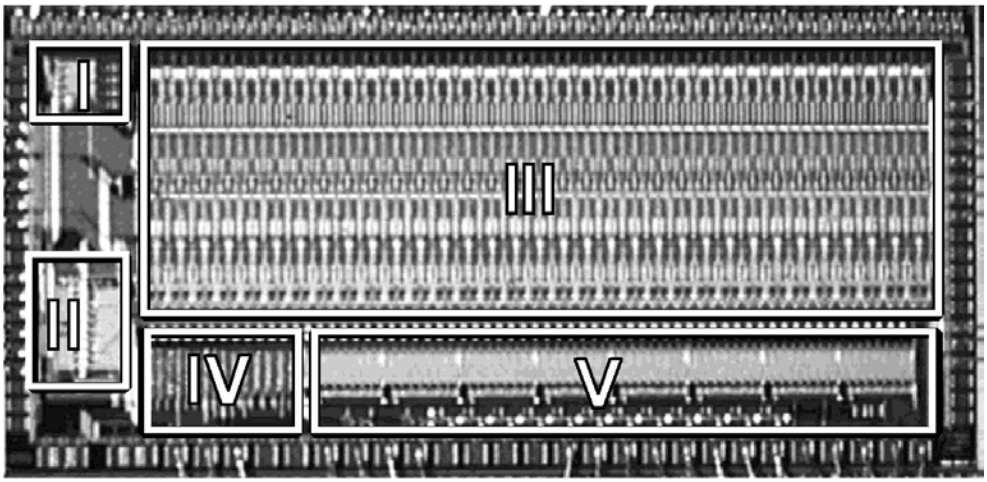


Fig. 3.13. Layout of the RX64 chip: I – calibration, II – bias DAC, III – 64 analogue channels, IV – control block, V – 64 counters

Due to matching concerns discussed earlier, special attention has been paid to minimise the channel-to-channel variation of the power supply voltages. The analogue power supply lines Vdd and Vss run across all channels and are nearly 6500 μm long and 250 μm wide. The lines are connected via triple bonding pads placed symmetrically on each side of the chip. These lines have been drawn using metal 2 layer that has resistance nearly twice lower than metal 1 layer. In order to avoid metal over the matched components (components of the feedback loops, differential pairs) and fit such wide lines close to the single-ended stages, an extra area inside the front-end channels has been added. These regions are filled with substrate or n-well contacts tied to appropriate lines. The digital power supply lines are only 80 μm wide, however, they are stacked of the metal 1 and metal 2 layers and connected with double bonding pads.

In additions to local guard rings surrounding PMOS and NMOS devices in the preamplifier and the shaper, there are two sets of global guard rings. One set of guard rings surrounds the whole analogue part while the second one encloses the whole digital part of the circuit. Guard rings for the analogue and the digital block have separate bonding pads.

Different parts of the RX64 IC have been designed using different techniques. Analogue front-end channels have been designed using full custom techniques, following the layout rules for good matching described in chapter 2. The layout of a single front-end channel is 80 μm wide and 1500 μm long. A fragment of the preamplifier layout with transistors M1–M4 of the folded cascode circuit, capacitor C1 and transistor M5 of the feedback loop is shown in Figure 3.14 (compare schematic in Figure 3.7). Two local guard rings: n-well ring and p+ring are also shown. The n-well ring surrounds the PMOS transistors and is tied to Vdd power supply line. The p+ ring is a set of substrate contacts which surrounds the NMOS transistors and is tied to Vss power supply line.

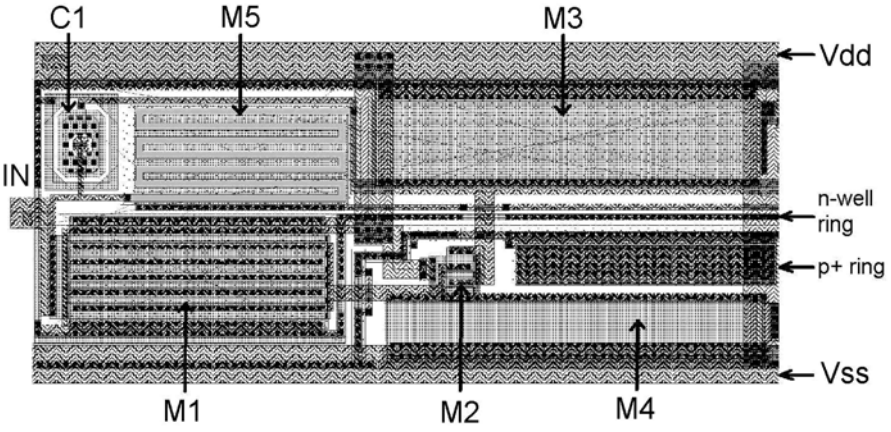


Fig. 3.14. Fragment of the preamplifier layout – compare with schematic in Figure 3.7

Full custom technique has also been used for design of the counter block with a main aim to minimise the area of this block. SPICE simulations have been performed on the transistor level and the layout has been optimised manually. Given a very regular structure of the counter block, this approach has appeared to be very effective, since the area of this block has been reduced by a factor of 2, compared to what could be achieved using the

standard cells and the automatic place and route techniques. After the layout extraction the SPICE simulations have been repeated again using the extracted netlist including the parasitics. In order to cover the variation of the process parameters, it is required that the circuit should pass the simulation for the nominal parameters at a frequency by a factor 2.5 higher compared to the nominal, i.e. at 25 MHz.

The control block, on the other hand, has a rather complicated logical structure while the total area of this block is small. Therefore, the only effective way to design such a block is to generate the scheme from the behavioural description and then use the standard cell place and route technique to generate the layout. The functional code for the control block has been written in the Verilog HDL language and then the scheme and the layout of the circuit have been generated automatically by the special parameterised procedures. Functional analysis of this block has been performed using Verilog simulation. The timing performance has been ensured by proper parameterisation of the standard cell delays.

3.9. Test results

The functionality and complexity of the RX64 design require that advanced testability functions are implemented on chip. Thanks to these features the chip can be fully tested, including functionality of digital part and measurements of analogue parameters of the front-end circuit, while controlled and read out only by a typical PC I/O card. Moreover, the tests can be performed every time, even for the chips assembled into multichip modules together with the silicon strip detector. In this chapter we present testability features of RX64, test results and some measurements which has been performed using X-ray sources.

3.9.1. Testability features

The basic functionality of the counters and the output readout circuit can be tested using a dedicated *CounterPulse* command. In response to this command a digital pulse is sent to the inputs of all counters.

A standard procedure for testing analogue circuits of architecture implemented in the RX64 design is to send a series of calibration pulses of a given amplitude to the test input (command *CalibrationPulse*) and to count the pulses at the output of the comparator. By scanning the comparator threshold and repeating this test for various amplitudes of the calibration signal, one can extract the gain and the noise of the analogue part of the front-end circuit, as well as the offset of the comparator for each channel [89]. To make easier above test, two DACs have been implemented in IC, one to control the amplitude of the internal calibration signals, and second to control the threshold of the comparator. Both of these DACs are set through the Control Block. It is worth noticing that one can measure the analogue parameters of the front-end circuit precisely while sending only digital command signals to the chip and receiving digital data from the chip. This aspect becomes very important because analogue calibration signals of amplitudes below 10 mV are needed, and bringing such low signals to the chip working in digital environment is not an easy task. Thus, all we need to test the chip fully is a PC I/O card which generates the clock signal and command sequences, and receives the data. As the typical I/O card generates TTL signals, and a TTL to LVDS signal translator needs to be implemented in the test set-up.

3.9.2. Basic functionality test

A first basic test, called the *Readout Test*, which checks the functionality of the digital part of the chip, is a sequence of two commands: *ReadoutNonDestructive* and *ReadoutDestructive*. The result of this test is a random pattern of the counter content, as set after powering the chip, since no power-up reset is implemented in the design. Response to the two above commands sent sequentially should be identical. Next step is to repeat the *ReadoutDestructive* command, and now in response one should receive all values equal 1. The next test, which allows one to verify the functionality of the counters, is the *Counting Test*. In this test the command *CounterPulse* is sent and the contents of the counters are checked each time using the *ReadoutNonDestructive* command. The RX64 prototype has proved to work correctly with respect to the *Readout Test* and the *Counting Test*.

3.9.3. DAC test

The next important function of the Control Block is loading the DACs. For all DACs the analogue output values can be measured on the dedicated probe pads. Thus, in the same test one can verify the functionality of that part of the Control Block which is responsible for the DAC loading, the interface circuit between the Control Block and the DACs, as well as the linearity of the DACs. All this circuit appears to be working correctly so it is possible to measure the response curves of the DACs. An example of such a test performed for the 8-bit DAC, which controls the comparator threshold, is shown in Figure 3.15. The plot shows the response curve of the DAC and the integral nonlinearity defined as

$$error_i = (V_{out-i} - V_{fit-i}) / a_F \tag{3.13}$$

where:

- $error_i$ – integral nonlinearity for i value at the input,
- V_{out-i} – output voltage corresponding to i value at the input,
- V_{fit-i} – value of the fitted straight line for i value at the input,
- a_F – fit slope.

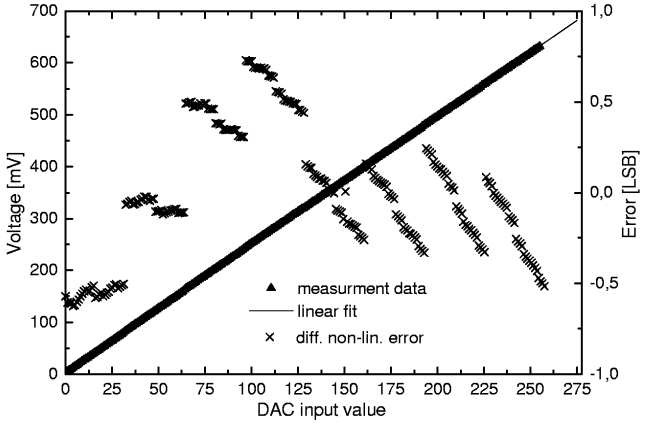


Fig. 3.15. Transfer characteristic and integral nonlinearity error of 8-bit threshold DAC

The error is expressed in the LBS units. As one can see, the errors are below the LBS value, and thus are completely acceptable for the foreseen chip application. The measured nonlinearity error is generated mainly in the current summing circuit based on the current mirror M66–M67 (Fig. 3.10). Due to the channel modulation effects, the effective ratio of the drain currents in M66 and M67 depends on drain-source voltages of both transistors, which are functions of the current fed into transistor M66 and the load resistance R_3.

3.9.4. Gain, noise and calibration

The binary architecture implemented in the RX64 chip has certain implications on the testing methods which have been used. A number of probe pads along the channel have been implemented so that basic functionality can be tested by probing the signals directly on the bare die. For routine measurements of the circuit parameters one has to assume that only the output of the discriminator is available. The basic analogue parameters, i.e. gain and noise can be obtained by scanning the threshold of the discriminator for given input signals. In this way one can measure integral pulse height spectrum at the discriminator outputs. If the noise is Gaussian, the integral pulse distribution is described by the error function. By differentiating the integral distribution one obtains the Gaussian distribution of which sigma is equal to the rms value of noise at the discriminator input. An example of measurements performed according to the procedures described above is shown in Figure 3.16.

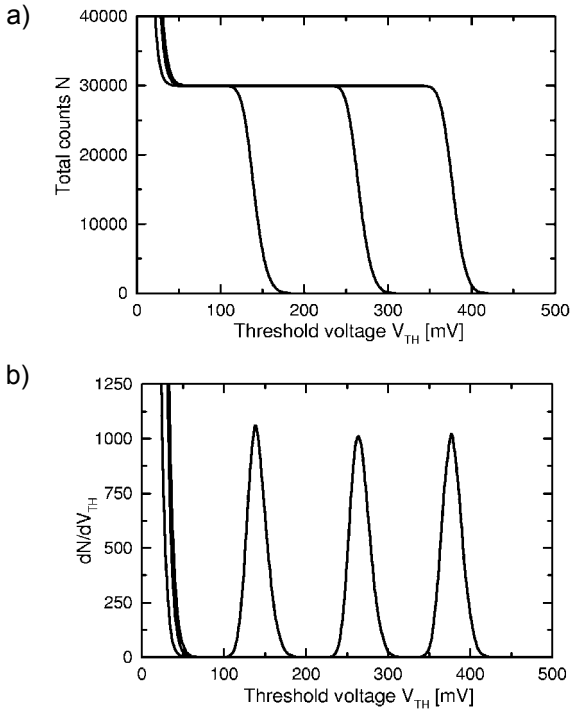


Fig. 3.16. Results of the threshold scan for three different input charges: a) measured integral pulse height spectrum; b) calculated differential pulse height spectrum

The threshold scans have been performed for three different values of the input charges injected to the calibration input of the preamplifier. The threshold values corresponding to the peaks of the differential pulse height spectrum (or mid points of the integral pulse height spectrum) determine the signal amplitudes at the discriminator input. Taking these measurements for the full range of the input signals, one can evaluate the gain, noise and linearity of the linear part of the circuit up to the discriminator. For the threshold values below 50 mV a rapid increase of noise counts is observed, as foreseen by formula (3.1).

Results of the measurements performed for the set-up with a silicon strip detector connected to the RX64 chip are summarised in Table 3.2. The total strip capacitance was about 2.5 pF and the leakage current was 60 pA per strip. The measurements have been performed for three different values of the IFEDSH current which controls the value of the feedback resistance in the shaper (g_{ds18} of transistor M18 – see Fig. 3.8) and thus the effective peaking time of the shaper.

Table 3.2
Gain and noise for various shaping time constants

Peaking time [μs]	Gain [μV/el.]	ENC [el. rms]
1.0	106.4	112
0.7	76.7	155
0.5	64.6	174

Considering the fact that this is a binary system, there is no particular requirement concerning the range of linearity, however, a wider linear range of the front-end circuit makes the calibration procedure of the system easier. An example of the full response curves of the RX64 chip is shown in Figure 3.17.

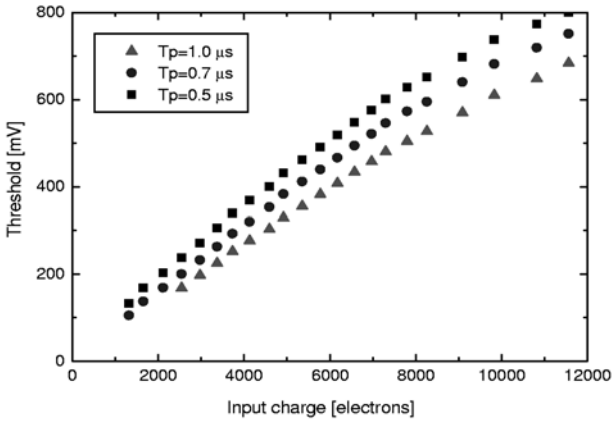
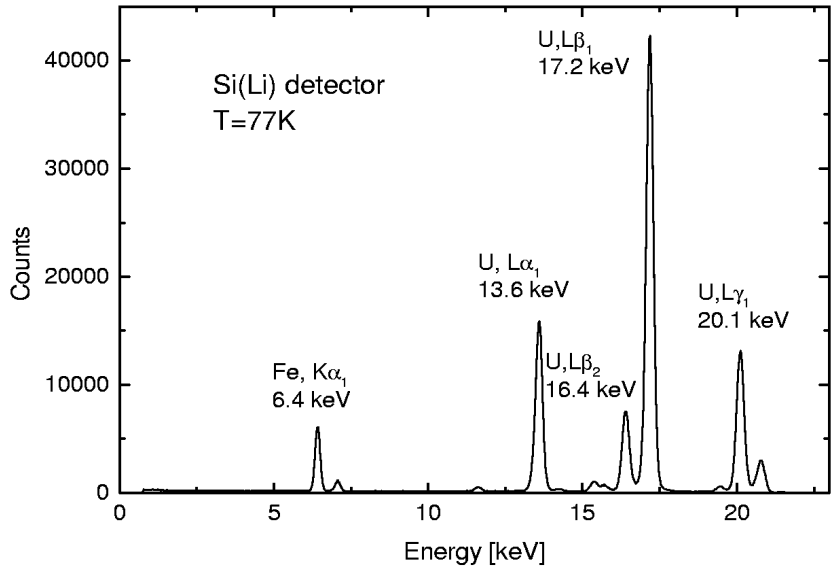


Fig. 3.17. Response curves of RX64 chip for three different shaping time constants

The circuit is sufficiently linear up to the input charge of 6000 electrons which corresponds to the X-ray energy range (deposited in silicon) up to 20 keV.

The presented measurements are sensitive to the absolute values of the test capacitors which depend on the processing parameters and therefore are not known accurately enough to be used for absolute calibration. In order to eliminate this uncertainty the system has been calibrated with low energy X-rays, assuming 3.67 eV for the generation of an electron-hole pair in silicon. A Pu-238 radioactive source, which generates three distinct X-ray lines 13.6 keV, 17.2 keV and 20.1 keV of comparable intensity, has been used. In addition, a fluorescent X-ray line of lower energy has been generated by inserting a copper or an iron foil between the source and the detector. Choosing proper thickness of the foil, according to the absorption coefficient and the fluorescence yield, one can obtain the intensity of the characteristic fluorescent radiation from the foil comparable to the intensity of the primary radiation from the source.

The spectrum has been measured using a high resolution Si(Li) spectrometer. It is used as a reference for further measurements with a silicon strip detector and our readout electronic system. The reference spectrum is shown in Figure 3.18. One should note that the measurements have been taken with the spectrometer cooled down to the liquid nitrogen temperature $T = 77$ K and with a shaping time constant of 10 μs.



3.18. Reference spectrum measured with a high resolution Si(Li) spectrometer

The 64 spectra measured using the developed ASIC RX64, connected to a strip detector working at room temperature, are shown in Figure 3.19a. The spectra have been obtained from integral distributions measured simultaneously for all 64 channels with the common threshold applied to all of them. Although the resolution of this system is not comparable with the resolution of the Si(Li) spectrometer, the four major peaks are clearly separated.

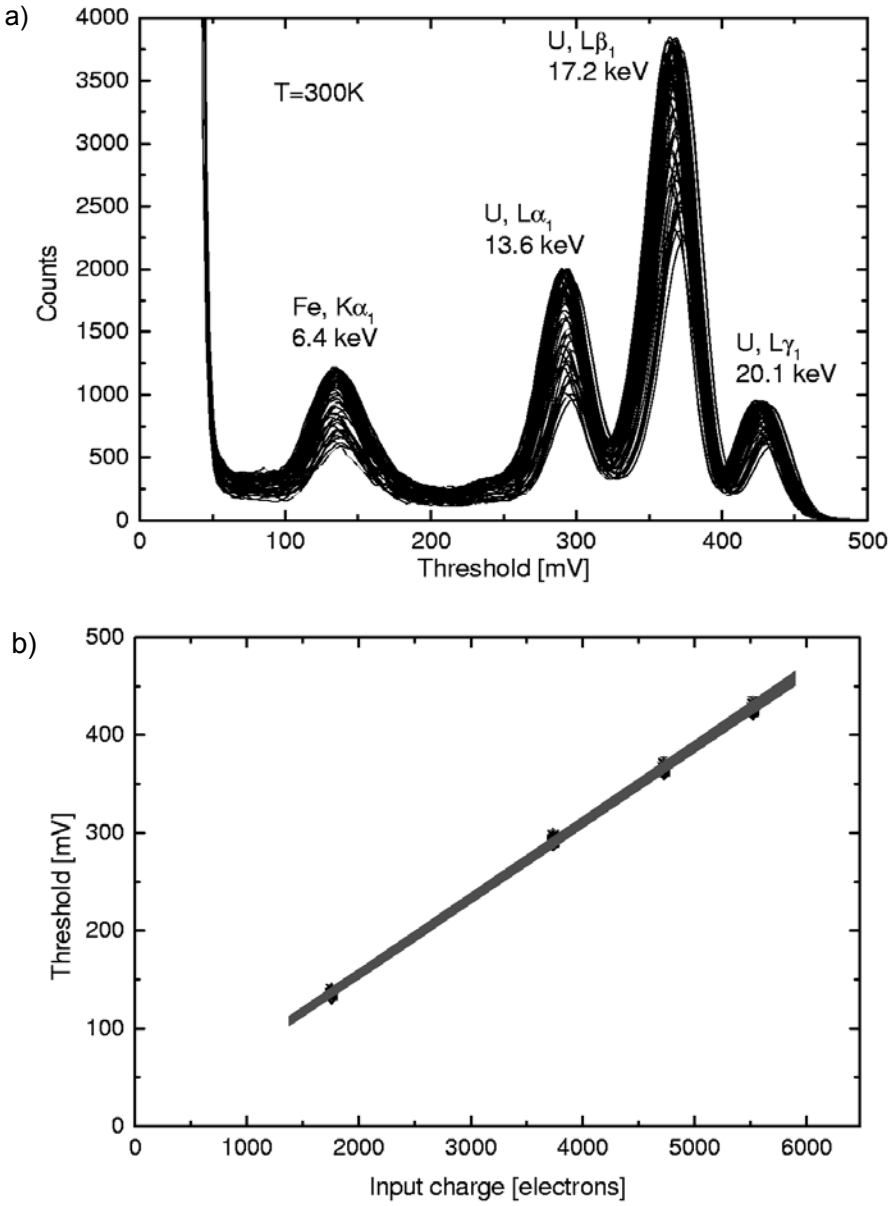


Fig. 3.19. Spectra of Pu-238 radioactive source and Fe Kα line measured with silicon strip detector and RX64 chip: a) spectrum for 64 channels; b) calibration and matching

The main factor which limits the resolution is the noise of the front-end electronics and shot noise of the detector leakage current. Another effect which limits the resolution in a strip detector is the charge sharing between the strips. The background which limits the

peak-to-valley ratio in the measured spectra comes from the events when the charge is divided between neighbouring strips. Relative heights of the peaks are different compared to the spectrum in Figure 3.18 due to the fact, that for a strip detector the detection efficiency decreases with the increasing energy of X-rays as the detector is only 300 μm thick. Differences in count numbers for various channels are due to the non-uniform radiation intensity across the detector. The obtained results show clearly that the energy resolution and the uniformity of parameters are sufficient for measuring X-rays of energy as low as 6.4 keV at room temperature.

The calibration lines for all 64 channels are overlaid on the plot in Figure 3.19b. From these plots one can calculate the gain and offsets for each channel, while from the width of the peaks in Figure 3.19a the ENC for each channel can be calculated. Typical distributions of these parameters for one RX64 IC are shown in Figure 3.20. These results have been obtained for the peaking time of 0.7 μs and the mean values are in good agreement with the electronic calibration (compare Table 3.2).

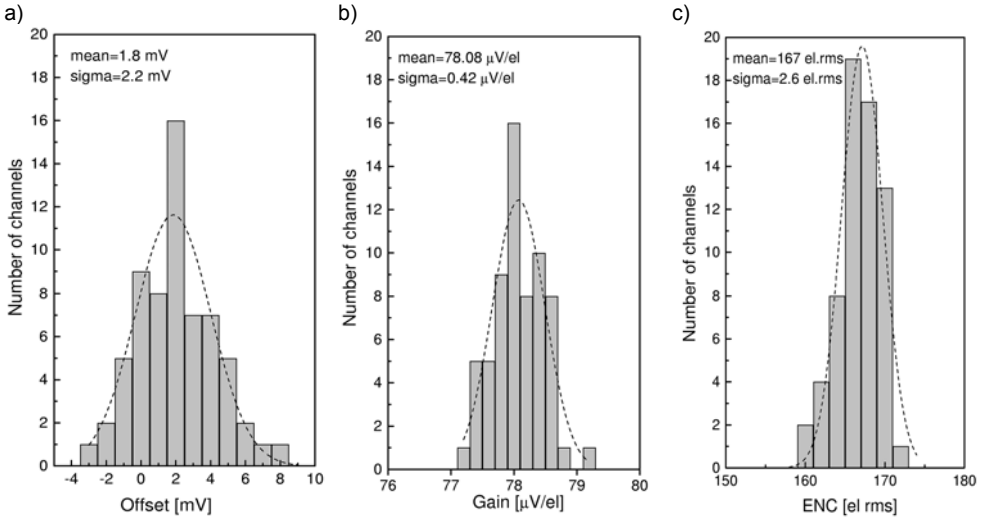


Fig. 3.20. Distributions of analogue parameters in 64 channels of one RX64 IC: a) discriminator offset; b) gain; c) equivalent noise charge

The spread of the discriminator offset is equal to 2.2 mV rms and, when referred to the input, it corresponds to 28 el. rms. This number is negligible compared to the equivalent input noise of 167 el. rms measured for this particular bias conditions of the RX64 IC and the silicon strip detector. This is smaller by almost a factor 4 compared to the noise and so it does not limit the performance of the system. The mean offset of 1.8 mV results from two effects: comparator hysteresis and transient response of the comparator. The comparator has hysteresis, which is symmetrical around the zero threshold, so it introduces a systematic offset. Secondly, as the calibration curves are measured using pulses and not DC voltages, the actual signal amplitudes must be higher than the DC threshold of the comparator in order to provide sufficient overdrive.

The spread of gain is small, about 0.5% on 1 sigma level. This is important as the effective threshold of the discriminator, in terms of the X-ray energy or the input charge to be discriminated, depends on the offset of the discriminator itself and on the gain of the amplifier. The contribution from the gain spread to the effective threshold spread is about 2.3 mV rms for the X-ray energy of 20 keV, which is the upper limit of the range foreseen in various applications.

Thus, in the worst case the spread of the effective threshold will be $\sqrt{2} \times 28$ el. rms, and it is still negligible compared to the ENC. For the ENC itself one can see quite good uniformity across the chip.

3.9.5. High counting rate characteristics

Another parameter important for many practical applications is the maximum counting rate. Taking into account a fully parallel architecture of the readout system, including the counters which serve as memory buffers, the counting rate considered for the total area of a detector depends on the detector segmentation. Regarding the counting rate limit for a single readout channel, there are two points to be taken into account.

First, in order to keep the noise contribution from the feedback resistor in the preamplifier within an acceptable range, this resistor has to be sufficiently large which results in a long discharge time of the feedback capacitance. At the high rate of signals this leads to piling-up of pulses at the preamplifier output and shifts of the DC operating points of the preamplifier. The other limitation occurs in the shaper where, although the tails of the pulses are much shorter compared to the preamplifier, their amplitudes are higher and at a certain rate of pulses the pile-ups start to degrade the resolution and eventually lead to losses of some fraction of pulses. The counting rate limit is not sharp and depends on the signal amplitude.

As discussed in section 3.4.1 the feedback resistor in the preamplifier is built as a long MOS transistor working in the linear region. This configuration provides a dynamic adjustment of the current discharging the feedback capacitor with increasing pulse rate. Since it is not easy to measure the signals directly at the preamplifier output, the principle of operation of this circuit is illustrated by the simulation results shown in Figure 3.21. The plots show the waveforms at the preamplifier output and the shaper output for two different rates of the input signals 20 kHz and 200 kHz. For the case of 200 kHz one can see the effect of the decrease of the DC potential at the preamplifier output and in result the increase of the V_{DS} across the feedback transistor. Consequently, we observe an increase of the discharge rate of the feedback capacitance. Due to this scheme, the circuit can handle much higher pulse rates compared to what one could expect from the small signal time constant of the preamplifier feedback network.

An example of the measurement which confirms the simulation results is shown in Figure 3.22. The plot shows an input staircase signal of 200 kHz applied to the calibration input of the preamplifier (CAL input, see Fig. 3.6) and the waveform measured at the comparator output. The amplitudes of the input signals correspond to the X-ray energy of 8 keV. It is important to note that for this measurement the input signal has to be in a form of a staircase instead of usually used rectangular pulses in order to avoid discharging of the feedback capacitor by pulses of reverse polarity generated by the falling edges of rectangular pulses.

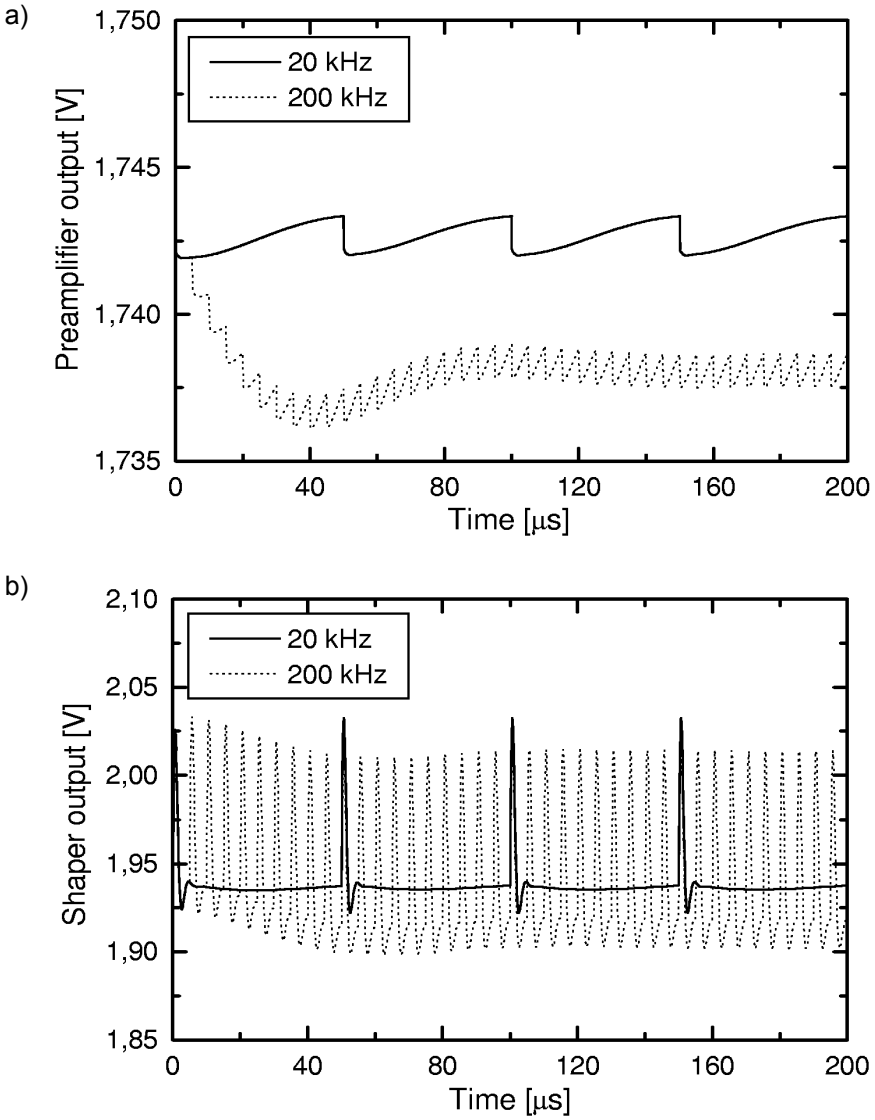


Fig. 3.21. Simulated waveforms for pulse rate of 20 kHz and 200 kHz: a) at the preamplifier output; b) at the shaper output

In order to characterise the high counting rate performance of the RX64 chip for signals arriving randomly, measurements have been performed for the module with a strip detector using X-rays from a tube with Cu target. We have measured gain, noise and efficiency as a function of average rate of X-ray photons absorbed in a single strip of the detector. The efficiency has been defined as a percent of pulses registered by the single readout electronics channel to the number of photons absorbed in a single strip of the detector.

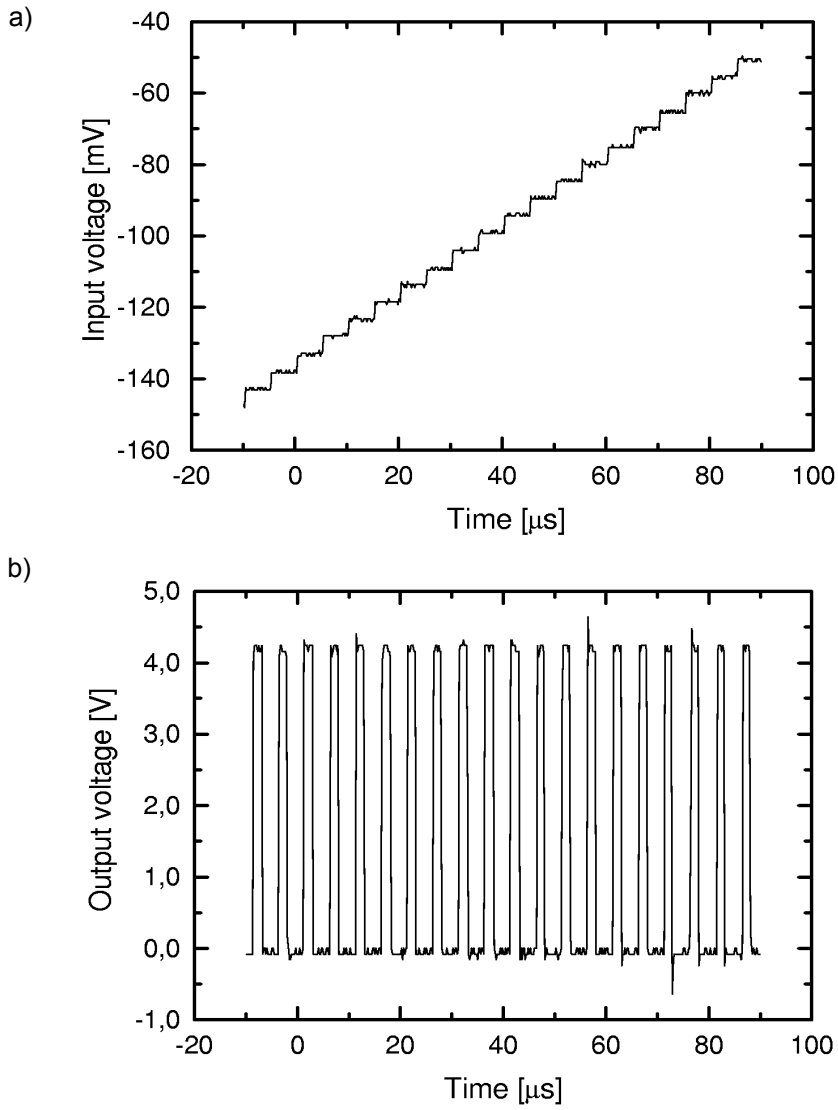


Fig. 3.22. Illustration of the operation of RX64 chip with the signal rate of 200 kHz: a) input signals applied to the test input of the preamplifier; b) waveform at the comparator output

Figure 3.23 shows the results of the measurements. All three parameters are degraded with increasing radiation rate. In the first approximation all these effects can be associated with the pile-ups in the preamplifier circuit. The ENC has been extracted from the width of the test pulse peak which has been measured simultaneously with the signals from the detector. The increase of the ENC in these measurements is caused mainly by gain fluctuations due to pile-up effects in the preamplifier and in the shaper.

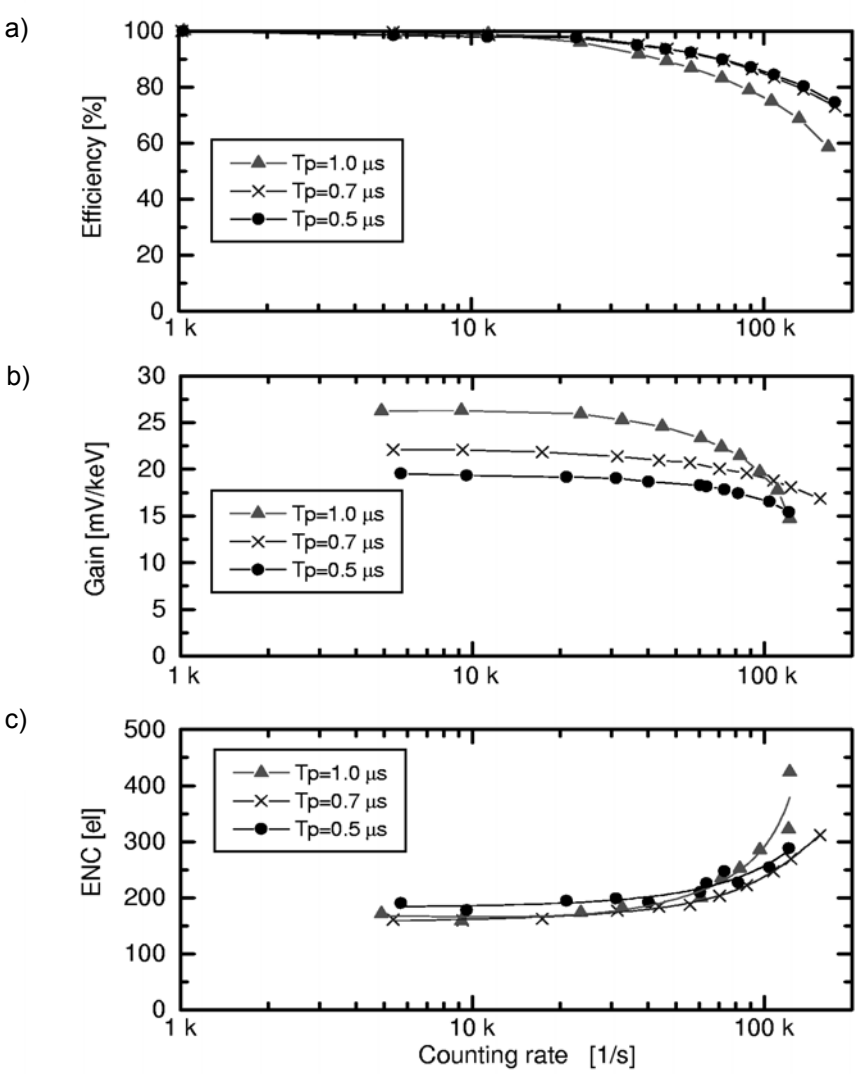


Fig. 3.23. High counting rate characteristic of RX64 chip: a) efficiency; b) effective gain; c) noise

3.10. Application of RX64 IC in position sensitive measurements at powder diffractometer

Since the RX64 IC meets the requirements of good analogue parameters and their uniformity from channel-to-channel is satisfactory, we have used it to build a low noise multichannel system for position sensitive measurements.

This system consists of one 128 strips silicon detector and two RX64 ICs. A central part of prototype module shown is in Figure 3.24. The module has been mounted at a powder diffractometer with Bragg-Bretano focusing [4] at the radius equal to 23 cm. The detector with 128 strips and a strip pitch 100 μm covers the angle of 3.16°.

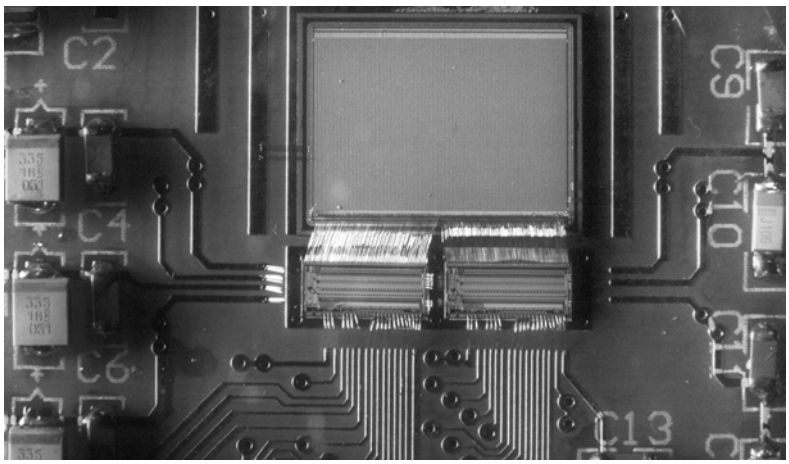


Fig. 3.24. Fragment of module for the measurement at θ-2θ diffractometer consisting of one 128-strip silicon detector and two RX64 ICs

In the first measurement the module has been kept in a fixed position and in one shot a quartz sample has been measured (Fig. 3.25). The plot shows a fragment of the diffractogram of quartz cluster at 68° where the separation of doublets for lines CuKα_1 = 8.047 keV and CuK α_2 = 8.027 keV is 0.19°.

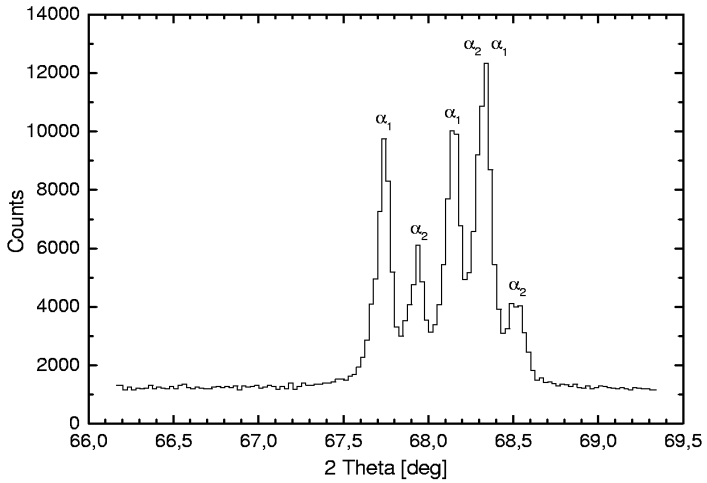


Fig. 3.25. Fragment of the diffractogram of quartz standard sample – measurement time 120 s

In the next measurement session the full diffraction pattern of silicon has been measured (Fig. 3.26). The diffractogram has been measured in 21 steps, each of 10 seconds. The spatial resolution is comparable with the resolution offered by the conventional detection system, including a moving slit and a proportional counter placed on the same arm, while the measurement time is reduced by two orders of magnitude, neglecting the time needed for the detector movement in the conventional system. The detection system with a silicon strip detector and the RX64 readout chip can handle count rates up to 10^5 counts/s for each strip independently.

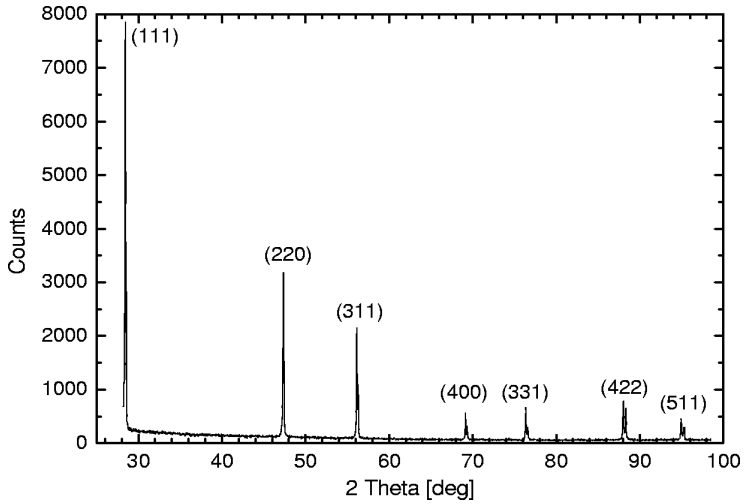


Fig. 3.26. Diffractogram of silicon – measurement time 21 steps × 10 s